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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/779,904 | 02/17/2004 | Masahiro Ishida | 02008.071003 | 9608 |

22511 7590 06/24/2009

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| EXAMINER | |
|---|---|
| LOUIE, OSCAR A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2436 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 06/24/2009 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/779,904 | ISHIDA ET AL. | |
| | Examiner | Art Unit | |
| | OSCAR A. LOUIE | 2436 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *4,16 and 27-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,16 and 27-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This non-final action is in response to the Request for Continued Examination filing of 04/13/2009. Claims 4, 16, & 17-33 are pending and have been considered as follows.

### *Examiner Note*

In light of the applicants' remarks and amendments, the examiner hereby withdraws his previous Claim Objections.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 4, 16, & 27-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugasawara (US-6043672-A) in view of Reynick (US-6714032-B1).

Claims 4 & 16:

Sugasawara discloses a fault analysis method of presuming a fault location of a semiconductor IC and a fault analysis apparatus configured to presume a fault location of a semiconductor IC comprising,

- "applying a power supply voltage to said semiconductor IC" (i.e. "A selectable power supply line for providing power to a particular section of the integrated circuit is activated by an enable signal provided to a selectable power supply switch coupled to the selectable power supply line") [column 3 lines 28-32];
- "supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC" (i.e. "Test development strategies include functional test wherein automatic test equipment (ATE) test programs are performed in which the circuit under test is stimulated with specified inputs while the outputs are monitored to determine if they correspond with simulated logic values") [column 1 lines 54-58];
- "the electrical potentials at the one or more locations are expected to change once the test pattern sequence is supplied" (i.e. "Defects in integrated circuits take many forms, some of which are test pattern sensitive…Quiescent current tests differ in that current is sensed rather than voltage, providing a simple means to monitor the entire circuit or portions thereof for over-current conditions") [column 1 lines 64-65 & column 2 lines 25-28];
- "measuring a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern" (i.e. "Once halted (i.e., no transistor state switching is occurring) the power supply of the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits") [column 2 lines 14-18];

- "determining whether said transient current shows abnormality or not" (i.e. "the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits. Such quiescent current tests are effective in detecting many faults that would otherwise not be found by other test strategies") [column 2 lines 16-20];
- "presuming a fault location out of said fault location list based on said test pattern sequence" (i.e. "This approach has typically included measuring current in a region of the integrated circuit, cutting lines to sections within the same region other than the section of interest, and then taking a additional measurements of current in the region") [column 2 lines 49-53];
- "the transient power supply current shows abnormality and said fault location list" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];
- "said transient power supply current is determined to be abnormal in a case that the time integral of said transient power supply current is over a predetermined value in said step of determining" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];

but, Sugasawara does not explicitly disclose,

- "storing a fault location list for the test pattern sequence," although Sugasawara does suggest an automated test equipment that would store test pattern sequences and which portions of the semiconductor integrated circuit have been isolated for testing, as recited below;
- "the fault location list includes one or more locations of components in said IC," although Sugasawara does suggest several components of a semiconductor integrated circuit that are tested for defects, as recited below;
- "said presuming comprises: deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality," although Reynick does suggest determining which circuits do not adhere to the signature criteria, as recited below;
- "presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location," although Reynick does suggest determining which circuits are defective, as recited below;

however, Sugasawara does disclose,

- "automated test equipment (ATE)" [column 5 line 11];

- "CMOS circuits use complementary p-channel metal-oxide-semiconductor field-effect (PMOS) transistors and n-channel metal-oxide-semiconductor field-effect (NMOS) transistors… Gate oxide defects, drain to source current leaks (punch-through), and p-n junction current leaks (such as drain or source to diffusion current leaks)" [column 1 lines 36-39, 66-67 & column 2 line 1];

whereas, Reynick does disclose,

- "In step 20, an experimental threshold current signature delta value is generated for a statistically valid set of known acceptable integrated circuits. In step 22, a current signature delta value is measured for a DUT. In step 24, the DUT current signature delta value is compared to the experimental threshold current signature delta value 20…" [column 7 lines 23-28];
- "…In step 26, a determination is made as to whether the current signature delta value of the DUT is greater than the experimental threshold current signature delta values. If the current signature delta value of the DUT are greater than the corresponding experimental threshold current signature delta value, the DUT can be identified as defective. Finally, in step 28, a further determination can be made as to whether a DUT which has a current signature delta value that is less than the corresponding experimental threshold current signature delta value, has a post-voltage stress current response for any of the set of measured vectors that is larger than a corresponding threshold post-voltage stress current response. If any post-voltage stress current response is greater than the corresponding

threshold post-voltage stress current response, the DUT can be identified as defective--even if the current signature delta values for the DUT are less than the experimental current signature delta values in step 26 …" [column 7 lines 28-45];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "storing a fault location list for the test pattern sequence" and "the fault location list includes one or more locations of components in said IC" and "said presuming comprises: deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality" and "presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location," in the invention as disclosed by Sugasawara since predetermined reference values or test limits would typically be stored within the testing device in order to be compared to the resulting value(s) and for the purposes of determining which circuits are defective in accordance with a set of signature pattern thresholds.

Claim 27:

Sugasawara discloses a fault analysis apparatus configured to presume a fault location of semiconductor IC comprising,

- "a power supply configured to apply a power supply voltage to said semiconductor IC" (i.e. "A selectable power supply line for providing power to a particular section of the integrated circuit is activated by an enable signal provided to a selectable power supply switch coupled to the selectable power supply line") [column 3 lines 28-32];

- "a test pattern sequence input unit configured to supply a test pattern sequence comprising a plurality of test patterns to said semiconductor IC" (i.e. "Test development strategies include functional test wherein automatic test equipment (ATE) test programs are performed in which the circuit under test is stimulated with specified inputs while the outputs are monitored to determine if they correspond with simulated logic values") [column 1 lines 54-58];
- "the electric potentials at the one or more locations are expected to change once the test pattern sequence is supplied" (i.e. "Defects in integrated circuits take many forms, some of which are test pattern sensitive…Quiescent current tests differ in that current is sensed rather than voltage, providing a simple means to monitor the entire circuit or portions thereof for over-current conditions") [column 1 lines 64-65 & column 2 lines 25-28];
- "an integral transient power supply current measuring unit configured to measure a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern" (i.e. "Once halted (i.e., no transistor state switching is occurring) the power supply of the device under test is measured by the ATE and the resulting value is compared to predetermined reference values or test limits") [column 2 lines 14-18];
- "a fault detector configured to determine that said transient power supply current is abnormal in a case that the time integral of said transient power supply current is over a predetermined value" (i.e. "the device under test is measured by the ATE and the

resulting value is compared to predetermined reference values or test limits. Such quiescent current tests are effective in detecting many faults that would otherwise not be found by other test strategies") [column 2 lines 16-20];

- "a fault location presuming unit configured to presume a fault location out of said fault location list based on said test pattern sequence" (i.e. "This approach has typically included measuring current in a region of the integrated circuit, cutting lines to sections within the same region other than the section of interest, and then taking a additional measurements of current in the region") [column 2 lines 49-53];
- "the transient power supply current shows abnormality and said fault location list" (i.e. "In order to isolate the defective area of an integrated circuit, a failure analysis engineer seeks to determine which section of the integrated circuit is responsible for unusual current levels") [column 2 lines 38-41];

but, Sugasawara does not explicitly disclose,

- "a fault location list memory unit configured to store a fault location list for the test pattern sequence," although Sugasawara does suggest an automated test equipment that would store test pattern sequences and which portions of the semiconductor integrated circuit have been isolated for testing, as recited below;
- "the fault location list includes one or more locations of components in said IC," although Sugasawara does suggest several components of a semiconductor integrated circuit that are tested for defects, as recited below;

- "said fault location presuming unit is configured to presume the fault location by: deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality," although Reynick does suggest determining which circuits do not adhere to the signature criteria, as recited below;
- "presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location," although Reynick does suggest determining which circuits are defective, as recited below;

however, Sugasawara does disclose,

- "automated test equipment (ATE)" [column 5 line 11];
- "CMOS circuits use complementary p-channel metal-oxide-semiconductor field-effect (PMOS) transistors and n-channel metal-oxide-semiconductor field-effect (NMOS) transistors… Gate oxide defects, drain to source current leaks (punch-through), and p-n junction current leaks (such as drain or source to diffusion current leaks)" [column 1 lines 36-39, 66-67 & column 2 line 1];

whereas, Reynick does disclose,

- "In step 20, an experimental threshold current signature delta value is generated for a statistically valid set of known acceptable integrated circuits. In step 22, a current signature delta value is measured for a DUT. In step 24, the DUT current signature delta

value is compared to the experimental threshold current signature delta value 20…" [column 7 lines 23-28];

- "…In step 26, a determination is made as to whether the current signature delta value of the DUT is greater than the experimental threshold current signature delta values. If the current signature delta value of the DUT are greater than the corresponding experimental threshold current signature delta value, the DUT can be identified as defective. Finally, in step 28, a further determination can be made as to whether a DUT which has a current signature delta value that is less than the corresponding experimental threshold current signature delta value, has a post-voltage stress current response for any of the set of measured vectors that is larger than a corresponding threshold post-voltage stress current response. If any post-voltage stress current response is greater than the corresponding threshold post-voltage stress current response, the DUT can be identified as defective--even if the current signature delta values for the DUT are less than the experimental current signature delta values in step 26 …" [column 7 lines 28-45];

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the applicant's invention to include, "a means for storing a fault location list for the test pattern sequence" and "a fault location list memory unit configured to store a fault location list for the test pattern sequence" and "said fault location presuming unit is configured to presume the fault location by: deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality" and "presuming a remaining analysis point out of the analysis points corresponding to the test pattern

sequence where the transient power supply current shows abnormality to be a fault location," in the invention as disclosed by Sugasawara since predetermined reference values or test limits would typically be stored within the testing device in order to be compared to the resulting value(s) and for the purposes of determining which circuits are defective in accordance with a set of signature pattern thresholds.

Claims 28-30:

Sugasawara and Reynick disclose a fault analysis method of presuming a fault location of a semiconductor IC, a fault analysis apparatus configured to presume a fault location of a semiconductor IC, and a fault analysis apparatus configured to presume a fault location of semiconductor IC, as in Claims 4, 16, & 27 above, their combination further comprising,

- "the semiconductor IC is a CMOS IC" (i.e. "To facilitate IC testing, many different IC testing methodologies have been developed. These testing methods have been developed for evaluating any of a number of types of ICs, such as complimentary metal-oxide semiconductor (CMOS) ICs…") [column 1 lines 40-43].

Claims 31-33:

Sugasawara and Reynick disclose a fault analysis method of presuming a fault location of a semiconductor IC, a fault analysis apparatus configured to presume a fault location of a semiconductor IC, and a fault analysis apparatus configured to presume a fault location of semiconductor IC, as in Claims 28-30 above, their combination further comprising,

- "the time integral of said transient power supply current is a sum of integrals of transient currents that flow in logic gates of the CMOS IC" (i.e. "…In the present invention, the base current signatures and the post-stress current signatures for the set of measured

vectors applied to the experimental ICs can be base quiescent current signatures and post-stress quiescent current signatures. The base current signatures and the post-stress current signatures for the set of measured vectors applied the experimental ICs can also be base transient current signatures and post-stress transient current signatures…") [column 9 lines 61-67 & column 10 lines 1-9].

***Response to Arguments***

3. Applicant's arguments with respect to claims 4, 16, & 27-33 have been considered but are moot in view of the new ground(s) of rejection as necessitated by the applicants' amendments.

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

a. Maly et al. (US-5025344) - built-in current testing of integrated circuits;

b. Sakaguchi (US-5949798) - integrated circuit fault testing system based on power spectrum analysis of power supply current;

c. Sanada (US-5864566) - Fault block detecting system using abnormal current and abnormal data output;

d. Sanada (US-5943346) - Fault point estimating system using abnormal current and potential contrast images;

e. Spica (US-6717428-B1) - method and apparatus for detecting defects in a circuit using spectral analysis of transient power supply voltage;

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2400 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/OAL/
06/19/2009
/David García Cervetti/
Primary Examiner, Art Unit 2436